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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
TRAN, MY CHAU T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/803,190	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MY-CHAU T. TRAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *2-5,8,9,12,13 and 15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7,10,11,14 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/26/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application and Claims Status

1. Applicant's amendment and response filed 10/26/2007, and the supplemental amendment filed 11/05/2007 are acknowledged and entered.

2. Claims 1-25 were pending. Applicants have amended claims 1, 7, 11, and 23-25 and added claims 26-31 in the amendment filed 10/26/2007; and in the supplemental amendment filed 11/05/2007, claim 11 is amended. No claims were cancelled. Therefore, claims 1-31 are currently pending. Claims 2-5, 8, 9, 12, 13, and 15-22 are drawn to non-elected species and/or inventions and thus these claims remain withdrawn from further consideration by the examiner, 37 CFR 1.142(b), there being no allowable generic claim. Accordingly, claims 1, 6, 7, 10, 11, 14, and 23-31 are under consideration in this Office Action.

Status of Claim(s) Objection(s) and /or Rejection(s)

3. The rejection of claims 1, 6, 7, 10, 23, and 24 under 35 USC 102(a) as being anticipated by EP 1310997 A2, now refers to as Udagawa et al., has been withdrawn in light of applicant's arguments (see pg. 19, second full paragraph, filed 10/26/2007).

4. The provisionally rejection under the judicially created doctrine of obviousness-type double patenting of claims 23 and 24 over claims 1, 2, 6, 7, 11, and 12 of copending Application No. 11/565,116 (US Patent Application Publication 2007/01266666 A1) has been withdrawn in view of the amendments of claims 23 and 24, i.e. the new limitation of '*wherein a first electrode of the first transistor is connected to the light emitting element, and wherein a second electrode*

of the first transistor is connected to the second transistor'. However, this rejection maybe reinstated if the new limitation is remove.

Maintained Rejection(s)

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1, 6, 7, 10, 11, 14, and 23-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishitoba et al. (US Patent 6,774,877).

For ***claims 1, 6, 7, 10, 11, 14, and 23-31***, Nishitoba et al. disclose an organic electroluminescent (EL) image display device (see e.g. Abstract; col. 1, lines 7-12; col. 3, line 49 thru col. 4, line 14; fig. 3). As illustrated by figure 3, the device comprises an organic EL element (ref. #11)(refers to instant claimed light emitting element/pixel electrode) and two transistors (ref. #8 and 9)(refers to instant claimed first and second transistors) connected to the organic EL element in a series (see e.g. col. 6, lines 17-59). The anode of the organic EL element (ref. #11) is connected to the drain (refers to instant claimed first electrode of the first transistor) of transistor (ref. #8)(refers to instant claimed first transistor) and the source (refers to instant claimed second electrode of the first transistor) of transistor (ref. #8) is connected to the drain of transistor (ref. #9)(refers to instant claimed second transistor) (see e.g. col. 6, lines 17-27; fig. 3). Additionally as illustrated by figure 3, the device comprise a switching transistor (ref. #12)(refers to instant claimed third transistor) wherein the drain (refers to instant claimed first electrode of the third transistor) is connected to the signal line (ref. #3) and the source (refers to

instant claimed second electrode of the third transistor) is connected to the gate electrodes of both transistors (ref. #8 and 9) (see e.g. col. 6, lines 28-36). The gates of the transistors (ref. #8 and 9) are connected to each others (refers to instant claimed gate electrodes) and they are p-channel MOS transistors (refers to instant claimed p-type transistor/same polarity)(see e.g. col. 6, lines 24-25 and 39-40; fig. 3). Nishitoba et al. disclose that the transistor (ref. #9) compensates the variations in the threshold voltage of the transistor (ref. #8) (see e.g. col. 6, lines 38-59). The transistor (ref. #8) operates in the saturation region, and the transistor (ref. #9) operates in the non-saturation region, i.e. linear region (see e.g. col. 6, lines 38-59). Nishitoba et al. also disclose that the channel width of transistors of references #6 to #9 is 4 μm, i.e. constant (see e.g. col. 7, lines 42-44). As shown in figure 6, there is a relationship between the channel length of transistors of references #7 and #9 and the variations in output current such that the desired characteristics can be obtained by selecting the channel length of transistors of references #7 and #9 according to the picture quality that is demanded of the image display device (see e.g. col. 6, lines 38-59; col. 7, lines 23-57), which imply that the size of the transistor's channel, i.e. length and width, would be a choice of experimental design and is considered within the purview of the cited prior art. Moreover, Nishitoba et al. disclose that the channel length of transistors of references #7 and #9 can be set to at least 0.5 times or at least one time but not greater than four times the channel length of transistors of references #6 and #8, i.e. if the channel length of transistor (ref. #9) is set at 15 μm then the channel length of transistor (ref. #8) is 7.5 μm such that the channel length of transistor (ref. #9) is 0.5 times that of the channel length of transistor (ref. #8) (see e.g. col. 7, lines 54-57).

For ***claims 11, and 25***, Nishitoba et al. disclose the method of driving the light emitting device wherein the step comprises controlling the current to be supplied to a light emitting device by the first and second transistors (see e.g. col. 3, line 49 thru col. 4, line 14; col. 6, line 60 thru col. 7, line 22; figs. 3 and 4).

Therefore, the device and method of Nishitoba et al. do anticipate the instant claimed invention.

Response to Arguments

7. Applicant's arguments directed to the above 102(e) rejection were considered but they are not persuasive for the following reasons. Please note that the above rejection has been modified from it original version to more clearly address applicant's newly amended and/or added claims and/or arguments.

[1] Applicant contends that Nishitoba et al. do not teach the limitation '*that a channel length of a first transistor is longer than a channel width thereof*'.

[2] Applicant alleges that '*varying the ratio of channel width to channel length has numerous potential effects on the overall function of the device*' for '*In the present invention, the size of the first transistor, i.e. the channel length and the channel width, is set such that the first transistor operates in a saturation region. In the case where a first transistor operates in a saturation region, the drain current Idl of the first transistor is calculated, for example, according to the formula "numeral 1" (page 8 of the present specification)*'.

Thus, the teachings of Nishitoba et al. do not anticipate the device and method of the instant claims.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. It is the examiner's position that Nishitoba et al. do teach the limitation '*that a channel length of a first transistor is longer than a channel width thereof*'. Nishitoba et al. disclose that the channel width of transistors of references #6 to #9 is 4 μm, i.e. constant (see e.g. col. 7, lines 42-44) and that the channel length of transistors of references #7 and #9 can be set to at least 0.5 times or at least one time but not greater than four times the channel length of transistors of references #6 and #8, i.e. if the channel length of transistor (ref. #9)(refers to instant claimed second transistor) is set at 15 μm then the channel length of transistor (ref. #8)(refers to instant claimed first transistor) is 7.5 μm such that the channel length of transistor (ref. #9) is 0.5 times that of the channel length of transistor (ref. #8) (see e.g. col. 7, lines 54-57). Accordingly, Nishitoba et al. do teach the limitation '*that a channel length of a first transistor is longer than a channel width thereof*'.

[2] The examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the effect of varying the ratio of channel width to channel length according to the formula "numeral 1" of pg. 8 of the present specification and paragraphs [0019] and [0020] of the present specification, pgs. 7-8) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Moreover, Nishitoba et al. disclose that the transistor (ref. #8)(refers to instant claimed first transistor) operates in the saturation region, and the transistor (ref. #9)(refers to instant claimed second transistor) operates in the non-saturation region, i.e. linear region (see e.g. col. 6, lines 38-59).

Therefore, the teachings of Nishitoba et al. do anticipate the device and method of the instant claims, and the rejection is maintained.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Although the examiner have cited some of applications for the rejection under nonstatutory double patenting (see below), it is noted that there are an enormous amount of applications and patents, which are commonly owned with the instant application, for the examiner to identify all applications and/or patents that can be rejected under nonstatutory double patenting. And as a result, applicants are requested to assist the Office in identifying all applications and/or patents that can be rejected under nonstatutory double patenting in regard to

the instant application, i.e. specifically for instant claims 1, 6, 7, 10, 11, 14, and 23-25, and especially instant claims 23-25.

10. Claims 23 and 24 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 3, 4, 7, 8, 11, 12, 15, and 16 of copending Application No. 11/208,278 (US Patent Application Publication 2006/0044229 A1). Although the conflicting claims are not identical, they are not patentably distinct from each other because both the instant claimed device and the device of copending Application No. 11/208,278 have similar structural features.

Specifically, the claimed device of claims 3 and 4 of copending Application No. 11/208,278 comprises a light emitting element (refers to instant claimed light emitting element/pixel electrode), a driving transistor (refers to instant claimed first transistor), and an AC transistor (refers to instant claimed second transistor). Both the driving transistor and the AC transistor are connected to the light emitting element and the power source line. The gate electrode of the AC transistor is connected to the power source line. As exemplified by figure 1, the gate electrode (refers to instant claimed second electrode of the first transistor) of the driving transistor is connected to the power source line and as a result it is connected to the gate electrode of the AC transistor. Claims 7 and 8 of copending Application No. 11/208,278 recite that both the driving transistor and the AC transistor have the same conductivity type (refers to instant claimed same polarity). Claims 11 and 12 of copending Application No. 11/208,278 recite that the driving transistor has a ratio channel length to channel width of 5 or more to 1.

Claims 15 and 16 of copending Application No. 11/208,278 recite that the AC transistor has channel length equal or shorter than the channel width.

That is the claimed device of the instant application is generic to the claimed device of copending Application No. 11/208,278 or in other word, claims 23 and 24 are anticipated by claims 3, 4, 7, 8, 11, 12, 15, and 16 of copending Application No. 11/208,278. Accordingly, the examined claims would be obvious over the claims of copending Application No. 11/208,278.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

11. Applicant's arguments directed to the above nonstatutory obviousness-type double patenting rejection were considered but they are not persuasive for the following reasons. Please note that the above rejection has been modified from it original version to more clearly address applicant's newly amended and/or added claims and/or arguments.

[1] '*Applicant respectfully requests that the double patenting rejections be held, in abeyance until an indication of allowable subject matter is made in either the present application or the copending applications. At such time, the Applicant will respond to any remaining double patenting rejections*'. See pg. 20 of the response filed 10/26/2007.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. In response to applicant request to held the provisional double patent in abeyance, the provisional rejection will not be held in abeyance (e.g., see MPEP § 804, subsection I.B. Between Copending Applications-Provisional Rejections, "*The 'provisional' double patenting rejection* ***should continue to be made by the examiner*** *in*

each application as long as there are conflicting claims in more than one application unless that "provisional" double patenting rejection is the only rejection remaining in one of the applications", and MPEP § 822.01). Here, a double patenting rejection is NOT the only rejection remaining in one of the applications and thus the double patenting rejection is proper. Thus, the provisional double patent rejection is maintained. Furthermore, applicant did not response to the request for assistance in identifying all applications and/or patents that can be rejected under nonstatutory double patenting in regard to the instant application, i.e. specifically for instant claims 1, 6, 7, 10, 11, 14, and 23-25, and especially instant claims 23-25 (see paragraph 10 above).

New Rejection(s) – Necessitated by Amendment

Claim Rejections - 35 USC § 112

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claims 1, 6, 7, 10, 11, 14, and 23-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. (This is a new matter rejection).

a. The amended claims 1, 7, 11, and 23-25 recite the limitations of a) '*a first electrode of the first transistor is connected to the light emitting element*', i.e. the

structural feature of the first transistor include a first electrode that is connected to the light emitting element; and b) '*a second electrode of the first transistor is connected to the second transistor*', i.e. the structural feature of the first transistor include a second electrode that is connected to the second transistor. These limitations, which narrows the structural features of the instant claimed first transistor, are not supported by the originally filed specification and/or claims; nor has applicant provided any indication where such support exists (i.e. applicant only states that '*Claims 1, 7, 11 and 23-25 have been amended to better recite the features of the present invention*', See pg. 15, lines 12-15 of response filed 10/26/2007). See MPEP § 714.02, 5th paragraph, last sentence; MPEP § 2163.02; and MPEP § 2163.06. Furthermore, the originally filed specification does not define the terms, i.e. '***a first electrode***' and '***a second electrode***', with regard to the claimed transistor since it is art recognize that the transistor includes three different electrodes, which are a gate electrode, a source electrode, and a drain electrode. For example, the instant specification, especially figures 2 and 4A, discloses a device with the driving transistor (ref. #202 and 402 of figs. 2 and 4A respectively) and the current control transistor (ref. #203 and 403 of figs. 2 and 4A respectively) that are connected to a power supply line (ref. #Vi) and the light emitting element (ref. #204 and 404 of figs. 2 and 4A respectively) (see pg. 12, lines 2-4 and pg. 16, lines 18-20). In both figures 2 and 4A, a source of the current control transistor (ref. #203 and 403 of figs. 2 and 4A respectively) is connected to the power supply line (ref. #Vi), and a drain of the driving transistor (ref. #202 and 402 of figs. 2 and 4A respectively) is connected to a pixel electrode of the light emitting element (ref. #204 and 404 of figs. 2 and 4A respectively)

(see pg. 12, lines 7-9 and pg. 16, lines 22-24). Additionally, although the original claims 1, 7, 11, and 23-25 recite that both the first and second transistors include gate electrode that are connected to each other, the originals claims does not recites the structural features of the first transistor wherein a) '*a first electrode of the first transistor is connected to the light emitting element*' and b) '*a second electrode of the first transistor is connected to the second transistor*'. Consequently, these limitations have no specification or original claim support, and it is considered new matter. If applicants disagree, applicant should present a detailed analysis as to why the claimed subject matter has clear support in the originally filed specification and/or claims.

b. New claims 26-31 recite the limitations of '*a first electrode of the third transistor is electrically connected to a signal line and a second electrode of the third transistor is electrically connected to the gate electrodes of the first transistor and the second transistor*'. These limitations, which narrows the structural features of the instant claimed third transistor, are not supported by the originally filed specification and/or claims; nor has applicant provided any indication where such support exists (i.e. applicant only states that '*new dependent claims 26-31 have been added to recite additional protection to which the Applicant is entitled*', See pg. 15, lines 12-15 of response filed 10/26/2007). See MPEP § 714.02, 5th paragraph, last sentence; MPEP § 2163.02; and MPEP § 2163.06. Furthermore, the originally filed specification does not define the terms, i.e. '***a first electrode***' and '***a second electrode***', with regard to the claimed transistor since it is art recognize that the transistor includes three different electrodes, which are a gate electrode, a source electrode, and a drain electrode. For example, the

instant specification, especially figures 2 and 4A, discloses a device wherein the gate electrode of the switching transistor (ref. #201 and 401 of figs. 2 and 4A respectively) is connected to the scanning line and one of either the source and the drain of the switching transistor is connected to the signal line while the other is connected to the gate line of the driving transistor (ref. #202 and 402 of figs. 2 and 4A respectively) and the current control transistor (ref. #203 and 403 of figs. 2 and 4A respectively) (see pg. 11, line 22 thru pg. 12, line 1 and pg. 16, lines 10-13). Additionally, although the original claims 4 and 5 recite a third transistor, the originals claims does not recites the structural features of the third transistor wherein '*a first electrode of the third transistor is electrically connected to a signal line and a second electrode of the third transistor is electrically connected to the gate electrodes of the first transistor and the second transistor*'. Accordingly, these limitations have no specification or original claim support, and it is considered new matter. If applicants disagree, applicant should present a detailed analysis as to why the claimed subject matter has clear support in the originally filed specification and/or claims.

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1, 6, 7, 10, 11, 14, and 23-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The amended claims 1, 7, 11, and 23-25 recite the limitation of '*a second electrode of the first transistor is connected to the second transistor*' which is vague and indefinite because it is unclear if the '*second electrode*' is synonymous with the instant claimed gate electrode. Claims 1, 7, 11, and 23-25 recite the limitation that the '*gate electrodes of the first transistor and the second transistor are connected to each other*'. Furthermore, the originally filed specification does not define the term of '*a second electrode*', with regard to the claimed transistor since it is art recognize that the transistor includes three different electrodes, which are a gate electrode, a source electrode, and a drain electrode. As a result, claims 1, 7, 11, and 23-25 and all its dependent claims are rejected under 35 U.S.C. 112, second paragraph.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Chau T. Tran whose telephone number is 571-272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/My-Chau T. Tran/
Patent Examiner
Art Unit 2629
January 22, 2008